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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,762	02/20/2004	Saar Drimer	X-1500 US	7414

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
12/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,762	DRIMER, SAAR	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10,12-20 and 22-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,12-20 and 22-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-2, 6-8 and 20-36 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. The drawings were received on October 01, 2007. These drawings are acceptable.

Claim Objections

3. Claims 6, 9-10, 14-19 and 22-36 are objected to because of the following informalities:

In claim 6, line 2, "based on" should be "is based on".

In claim 9, line 12, a comma "," should be inserted after the word "data".

In claim 16, line 2, "output it to" should be "output the data to". The dependent claims 10, 14-15 and 17-19 depend either directly or indirectly from claim 9.

In claim 22, line 5, "an error" should be "the error".

In claim 31, line 8, "convert it from" should be "convert the predetermined source data from".

In claim 35, line 4, "of the" should be "of the jitter".

The dependent claims 23-30, 32-34 and 36 depend either directly or indirectly from claim 22.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 14-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 14 recites that the transceiver, the jitter performance tester, and the extraction circuit are embedded within a programmable logic device. However, as shown in Figure 3 and discussed in the specification of the present invention, wherein the extraction circuit comprises at least part of a RN generator 392 and a sample 394, clearly, the RN generator 392 and the sample 394 are not embedded within the programmable logic device 350. The dependent claims 15-17 depend either directly or indirectly from claim 14.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 4-10, 12-20 and 22-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lesea et al., U. S. Patent No. 7,218,670 (hereinafter "Lesea") in view of Wallace, U. S. Patent No. 5,633,816.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Lesea discloses a communication system in Fig. 4 comprising a programmable logic device 450, an external clock source 438, a serial output 476, and a host programmer 490. Clearly the block elements within the programmable logic device 450, the external clock source 438, the serial output 476, and the host programmer 490 are identical to the block elements within the programmable logic device 350, the external clock source 338, the serial output 376, and the host programmer 390 of Figure 3 of the present invention as recited in claims 1-2, 4-10, 14-16, 20 and 22-36.

Regarding claims 1, 7, 12-13, and 17-20, Lesea fails to show or suggest that a RN generator 392 or a sampling circuit 394 is coupled to the counter 366 of the programmable logic device 450, for example, a sampler to sample at least a portion of the bits of the counter to define the random number as recited in claim 1; wherein the extraction circuit comprises a sampler to sample at least a portion of an output of the jitter performance tester as recited in claim 7; the extraction circuit to enable the sampler once every counter duration as recited in claim 12; the extraction circuit operable to control length of the durations as recited in claim 13; a RS-232 interface to sample at least a portion of the counter, with a sampling rate less than a data transfer rate of the transmitter as recited in claim 17; the extraction circuit is operable to define the random numbers based upon a number of bit differences determined by the comparator as recited in claim 18; the extraction circuit is operable to define the random numbers based upon the respective durations required to produce a predetermined number of difference counts as determined by the comparator and the counter as recited in claim 119; and the steps of sampling at least a portion of the counting over a

duration and defining the random number based on the sampling over the duration as recited in claim 20.

Wallace discloses a random number generator circuit 100 in Figure 2 which generates random numbers 104 to a processor 206 through a bus interface 202. Figure 3 shows a block diagram illustrating the bus interface circuit 202 of Figure 2. The detailed embodiment of the random number generator 100 is shown in Figure 1 which comprises a shift register (or counter) 101 to receive a feedback data b_f based on the timing of a system clock SYSCLK to generate the random numbers 104, and a summing circuit to add bits 3 and 15 of the shift register 101 to output the feedback data b_f. Wallace also teaches that a sampling circuitry provides a least a portion of shift register bits as one of the sequence of random numbers. Abstract and Col. 1, lines 56-59.

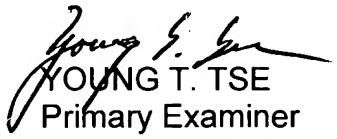
Therefore, it would have been obvious to one of ordinary skill in the art to include a sampling circuit or extraction circuit, for example, coupled to the output of Lesea's counter 366 as taught by Wallace in order to provide a portion of the counter bits to generate a portion of the random numbers over the durations of the system clock, as recited in claim 1, 7, 12-13, and 18-20.

Regarding claim 17, since the sampling circuitry generates a portion of the counter bits of the random numbers and the data transfer rate of the counter is the same as the data transfer rate of the transmitter, obviously sampling rate of the sampling circuitry is less than the data transfer rate of the transmitter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



YOUNG T. TSE
Primary Examiner
Art Unit 2611